

4/PPTS

INTEGRATED CIRCUIT ARRANGEMENT AND METHOD FOR THE MANUFACTURE THEREOF

The question of planarity is increasingly gaining in significance in the realization of integrated circuit arrangements having high packing density and, in particular, having structural sizes below 0.25 μm . In the manufacture of the integrated circuit arrangement, useful structures that have a circuit-oriented function in the circuit arrangement are generated on a semiconductor substrate. Such useful structures are, for example, terminal electrodes, gate electrodes or interconnects. These useful structures are respectively manufactured in planes by structuring a previously produced layer. Insulation layers are provided between successive planes. These insulation layers are planarized by polishing and/or etching.

The planarity that can be achieved when planarizing layers is thereby dependent on the geometrical density of the useful structures in the respective plane. Given an extremely non-uniform occupation with useful structures, large spaces locally derive wherein irregularities occur in the planarization process. It has therefore been proposed (see, for example, D. Widmann, H. Mader, H. Friedrich, *Technologie Hochintegrierter Schaltungen*, 2nd Edition, Springer-VErlag, 1996, pages 346 through 347) to insert filling structures between the useful structures that have no circuit-oriented function but that nonetheless increase the local geometrical density. As a result thereof, a uniform occupation in the respective plane is assured, this enabling a higher planarity following planarization steps.

When the useful structures and the filler structures are composed of conductive material, then a charging of the filler structures can occur during operation. In order to avoid this, the filler structures are applied to a fixed potential, as disclosed in Widmann et al. This contacting ensues via a specific wiring that is arranged in a metallization planes [sic] arranged above the useful and filler structures. This additional wiring and the contacts between the additional wiring and the filler structures makes the production of the layout more difficult.

The invention is based on the problem of specifying an integrated circuit arrangement that can be manufactured with high planarity, whereby a charging of electrically conductive filler structures is avoided and for which the layout can be produced with reduced outlay. Further, a method should be recited for manufacturing such a circuit arrangement.

5 This problem is inventively solved by an integrated circuit arrangement according to claim 1 as well as by a method for the manufacture thereof according to claim 8. Further developments of the invention proceed from the remaining claims.

A doped region is provided in a semiconductor substrate in the integrated circuit arrangement. A plane with conductive useful structures and at least one conductive filler structure is arranged at the surface of the semiconductor substrate. The conductive useful structures are, for example, terminal electrodes, gate electrodes, interconnect sections, wirings or the like. The conductive filler structure is conductively connected to the doped region. For example, the substrate body itself or 10 a doped well in which active components are arranged is suitable as doped region. The substrate body and/or the doped well in which components are arranged are already charged with a fixed supply voltage in integrated circuit arrangements during operation. The connection to the conductive filler structure assures that the conductive filler structure also lies at this potential. Since the doped well or the 15 substrate body are already connected to fixed potential, the additional wiring that is only provided for the purpose of connecting the filler structures can be omitted in the inventive integrated circuit arrangement. The layout is thus simplified. In particular, it can be produced by automatic layout generation. The position of the filler structure can be determined program-controlled.

20 The electrical connection of the conductive filler structure to the doped region preferably ensues via a via hole and a contact. The via hole overlaps the conductive filler structure and the doped region, so that the surface of the conductive filler structure and of the doped region are in communication with the contact. The via hole and the contact are preferably produced simultaneously with via holes and 25

contacts to conductive useful structures. No additional process steps are therefore required for this purpose.

Since only extremely slight current (chargeings, capacitative shift currents, etc.) need be eliminated, an overlapping contact is not compulsory. On principle, the 5 side wall contact surface already suffices. Other high-impedance eliminations via components are suitable for this purpose.

For example, a MOS (completely or partially activated), two anti-polar connected diodes or the like are suitable as components for connection between the conductive filler structure and the doped region. They are realized, for example, in 10 that the filler structure is conducted beyond the insulation zone and is connected to the useful structure with a contact, for example a junction.

It lies within the scope of the invention to arrange a metallization level above the plane wherein the conductive filler structure is arranged and to connect the filler structure to the metallization level to which the filler structure is connected via 15 the further contact lies at the same potential as the doped region during operation. The contact and the further contact then form an additional integrated contact for the doped region.

The plane in which the conductive filler structure is arranged can be either a gate plane that is arranged in the proximity of the surface of the semiconductor 20 substrate or a metallization plane that is arranged above the gate plane and/or further metallization planes.

For manufacturing the integrated circuit arrangement, a doped region is formed in the semiconductor substrate. The plane with conductive useful structures and at least one conductive filler structure is formed on the semiconductor substrate 25 by application and structuring of a conductive layer. An insulation structure is generated that surrounds the conductive useful structures and the conductive filler structure and covers them. Since the conductive useful structures and the conductive filler structure are formed of the conductive layer, they exhibit essentially the same height. The connection between the doped region and the conductive filler structure

is preferably produced by opening a via hole, which overlaps the conductive filler structure and the doped region, and by formation of a contact.

It lies within the scope of the invention to employ a monocrystalline silicon wafer, the monocrystalline silicon layer of a SOI substrate with a carrier wafer, 5 an insulating layer and a monocrystalline silicon layer or a substrate that contains SiC as semiconductor substrate.

The connection of the conductive filler structure to the doped region can be alternatively undertaken via a local wiring level. What is referred to as local wiring level is an electrically conductive connection that is effective in the lateral 10 environment. Local wiring levels are formed, for example, of $TiSi_2$ in the form of strip-shaped conductors, what is referred to as a $TiSi_2$ strap.

When the plane in which the conductive filler structure is arranged is the gate plane, the conductive useful structures contain gate electrodes. The gate electrodes can be formed either by structuring a conductive layer, from which the 15 conductive filler structure is then formed, or by structuring a plurality of sub-layers.

It lies within the scope of the invention that that part of the doped region that is overlapped by the via hole for connection to the conductive filler structure are [sic] separated from parts of the doped region wherein active elements of the circuit arrangement are arranged, being separated therefrom by an insulation structure, for 20 example a trench filled with insulating material. In this case, the doped region extends more deeply into the substrate than the insulation structure. As a result thereof, shorts between active elements and the contact are avoided.

The invention is explained in greater detail below with reference to an exemplary embodiment shown in the figures.

25 Figure 1 shows a section through a semiconductor substrate with insulation regions and a doped well.

Figure 2 shows the section through the semiconductor substrate after formation of a gate oxide and deposition of a conductive layer.

Figure 3 shows the section through the semiconductor substrate after structuring the conductive layer for forming conductive useful structures and conductive filler structures and after formation of source/drain regions and a well contact.

5 Figure 4 shows the section through the semiconductor substrate after formation of a planarizing insulation layer.

Figure 5 shows the section through the semiconductor substrate after formation of an intermediate oxide layer.

10 Figure 6 shows the section through the semiconductor substrate after formation of via holes and contacts.

Figure 7 shows the section through the semiconductor substrate after formation of a metallization level and a further contact between the conductive filler structure and the metallization level.

The illustrations in the figures are not to scale.

15 Insulation trenches 2 are formed in the surface of a substrate 1 of monocrystalline silicon by etching trenches and filling the trenches with insulating material (see Figure 1). The filling of the insulation trenches ensues by planarizing steps, for example by chemical-mechanical polishing. Subsequently, a masked ion implantation for formation of a p-doped well 3 is implemented upon employment of 20 photolithographic process steps. The doped well 3 is doped, for example, with boron and a dopant concentration of 5×10^{17} at/cm³.

The doped well 3 comprises a greater depth than the insulation trenches 2. The doped well 3 is laterally surrounded by one of the insulation trenches 2. A further insulation trench 2 is arranged such within the doped well 3 that the doped well 3 25 adjoins the surface of the substrate 1 in an active region 4 and in a terminal region 5. The active region 4 is provided for the acceptance of active elements.

The depth of the doped well 3 amounts, for example, to 1 μ m. The depth of the insulation trenches 2 amounts, for example to 400 nm.

Subsequently, a gate oxide 6 is formed, for example by thermal oxidation (see Figure 2). The gate oxide 6, for example, is formed in a layer thickness of 6 nm. Subsequently, a conductive layer 7 is deposited. Any material that is suitable for formation of gate electrodes is suitable for the conductive layer 7, particularly doped polysilicon, metal silicide, TiN. The conductive layer 7 is formed in a layer thickness of, for example, 200 nm.

Upon employment of photolithographic process steps, the conductive layer 7 is structured such that conductive useful structures 71 and conductive filler structures 72 are formed therefrom (see Figure 3). The conductive useful structures 71 are, for example, gate electrodes. The conductive filler structures 72 have no circuit-oriented function. They are arranged such that a uniform geometrical occupation by the conductive useful structures and the conductive filler structures is established.

SiO_2 spacers 8 are formed at the side walls of the conductive useful structures 71 and of the conductive filler structure 72 by conformal deposition and anisotropic re-etching of a SiO_2 layer.

Source/drain regions 9 are formed self-aligned relative to the conductive useful structure 71 by masked ion implantation wherein the surface of the active region 4 is uncovered but the surface of the terminal region 5 is covered. The source/drain regions 9 are, for example, doped with arsenic or phosphorous and comprise a dopant concentration of 8×10^{19} at/cm³.

Upon employment of a further mask, which covers the active region 4 but leaves the terminal region 5 uncovered, a well contact 10 is subsequently formed. The well contact 10 is doped, for example, with boron and comprises a dopant concentration of 6×10^{19} at/cm³.

Subsequently, a planarizing insulation layer 11 is formed, this being ground back to such an extent by chemical-mechanical polishing that it terminates in height with the conductive useful structure 71 and the conductive filler structures 72 (see Figure 4). When planarizing the planarizing insulation layer 11, the conductive

useful structure 71 and the conductive filler structures 72 act as planarization supporting points.

Subsequently, a first intermediate oxide layer 12 is deposited. Via holes to the source/drain regions 9, to the conductive useful structure 71 and to the well contact 10 and the neighboring, conductive filler structures 72 are subsequently etched with the assistance of photolithographic process steps and anisotropic dry etching (see Figure 6). By filling the via holes with metal, for example tungsten, contacts 131 to the source/drain regions 9 and the conductive useful structure 71 and an overlapping contact 132 to the well contact 10 and the neighboring, conductive filler structures 72 are formed (see Figure 6). The overlapping contact 132 is in communication both with the surface of the neighboring, conductive filler structures 72 as well as with the surface of the well contact. As a result thereof, the filler structures 72 are connected to the doped well 3 via the well contact 10.

Alternatively, the overlapping contact 132 is arranged such that it meets the surface of the substrate 1. In this case, a substrate contact is formed at the surface of the substrate 1 by implantation with dopant, which effects the same conductivity type that the substrate comprises.

Subsequently, a second intermediate oxide layer 14 is deposited wherein a further via hole that meets the overlapping contact 132 is opened. The further via hole is filled with a further contact 15, for example, of tungsten. Finally, a metallization level 16 is formed that is in communication with the further contact 15 (see Figure 7). The metallization level 16 is applied to the same potential as the doped well 3 during operation of the circuit arrangement.